IN THE CLAIMS:

Please amend claims 1, 17, 25, 31, 33, and 37, as set forth below. Also, please cancel claims 28-30 and add new claims 49-63. Please note that all claims currently pending in the application are included below for clarity, and a marked up version of the claims is appended at the end of this response.

1. (Twice Amended) A thermal management system located on an integrated circuit die comprising:

a temperature detection element formed directly on an integrated circuit die, the temperature detection element including at least one temperature sensor having an output;

a power modulation element formed directly on the integrated circuit die, the power modulation element to reduce power consumption of the integrated circuit die in response to the output of the at least one temperature sensor;

a control element formed directly on the integrated circuit die, the control element including at least one register to provide an enable/disable bit for the thermal management system; and

a visibility element formed directly on the integrated circuit die, the visibility element to indicate a status of the output of the at least one temperature sensor.

2. (Amended) The system of claim 1, the at least one temperature sensor comprising:

a reference voltage source providing a reference voltage;

a programmable voltage source providing a programmable voltage proportional to a temperature of the integrated circuit die; and

a comparator having one input coupled via a first signal line to the reference voltage source and another input coupled via a second signal line to the programmable voltage source, the comparator to provide a signal at the output of the at least one temperature sensor in response to the programmable voltage substantially equaling the reference voltage.

3. (Amended) The system of claim 2, further comprising a pulse dampener coupled to the first signal line, the pulse dampener to at least partially remove electrical noise from the reference voltage.

4. (Amended) The system of claim 2, further comprising an analog filter coupled to the second signal line and the first signal line, the analog filter to detect voltage spikes present in the reference voltage and to add substantially identical voltage spikes to the programmable voltage.

5. (Amended) The system of claim 2, further comprising a digital filter coupled to an output of the comparator, the digital filter including an up-down counter to count clock pulses, the up-down counter to increment once for each clock pulse detected when the comparator output is at a first state and to decrement once for each clock pulse detected when the comparator output is at a second state.

6. (Amended) The system of claim 1, the control element further including at least one of a register to selectively disengage a specified portion of the thermal management system, a register to enable the thermal management system in response to an occurrence of an external event, a register to force the thermal management system active while overriding a disable bit provided by the at least one register, and a register to allow external software and hardware to enable the thermal management system.

7. (Amended) The system of claim 1, the visibility element including at least one of a register to indicate the status of the temperature sensor output, a register to provide a sticky bit, a counter to count a number of lost clock cycles resulting from operation of the thermal management system, and circuitry to generate an interrupt when the output of the at least one temperature sensor transitions to a different state.

8. (Amended) The system of claim 1, the power modulation element to reduce the power consumption of the integrated circuit die by performing at least one of lowering a supply voltage to the integrated circuit die, lowering a frequency of a clock signal provided by internal clock circuitry on the integrated circuit die, performing clock gating of the clock signal provided by the internal clock circuitry, performing clock throttling of the clock signal provided by the internal clock circuitry, selectively blocking clock pulses of the clock signal provided by the internal clock circuitry, disabling at least one of a plurality of functional units on the integrated circuit die, limiting instructions sent to at least one of the plurality of functional units on the integrated circuit die, and changing a behavior of at least one of the plurality of functional units on the integrated circuit die.

9. (Amended) A microprocessor comprising:

a die having a plurality of functional units formed thereon;

internal clock circuitry formed on the die and coupled to at least one of the plurality of functional units; and

a thermal management system formed directly on the die, the thermal management system including

a temperature detection element including at least one temperature sensor having an output;

a power modulation element to reduce power consumption of at least one of the functional units in response to the output of the at least one temperature sensor;

a control element including at least one register to provide an enable/disable bit for the thermal management system; and

a visibility element to indicate a status of the output of the at least one temperature sensor.

10. (Amended) The microprocessor of claim 9, the at least one temperature sensor comprising:

a reference voltage source providing a reference voltage;

a programmable voltage source providing a programmable voltage proportional to a temperature of the die; and

a comparator having one input coupled via a first signal line to the reference voltage source and another input coupled via a second signal line to the programmable voltage source, the comparator to provide a signal at the output of the at least one temperature sensor in response to the programmable voltage substantially equaling the reference voltage.

11. (Amended) The microprocessor of claim 10, further comprising a pulse dampener coupled to the first signal line, the pulse dampener to at least partially remove electrical noise from the reference voltage.

12. (Amended) The microprocessor of claim 10, further comprising an analog filter coupled to the second signal line and the first signal line, the analog filter to detect voltage spikes present in the reference voltage and to add substantially identical voltage spikes to the programmable voltage.

13. (Amended) The microprocessor of claim 10, further comprising a digital filter coupled to an output of the comparator, the digital filter including an up-down counter to count clock pulses, the up-down counter to increment once for each clock pulse detected when the comparator output is at a first state and to decrement once for each clock pulse detected when the comparator output is at a second state.

14. (Amended) The microprocessor of claim 9, the control element further including at least one of a register to selectively disengage a specified portion of the thermal management system, a register to enable the thermal management system in response to an occurrence of an external event, a register to force the thermal management system active while overriding a disable bit provided by the at least one register, and a register to allow external software and hardware to enable the thermal management system.

15. (Amended) The microprocessor of claim 9, the visibility element including at least one of a register to indicate the status of the temperature sensor output, a register to provide a sticky bit, a counter to count a number of lost clock cycles resulting from operation of the thermal management system, and circuitry to generate an interrupt when the output of the at least one temperature sensor transitions to a different state.

16. (Amended) The microprocessor of claim 9, the power modulation element to reduce the power consumption of the at least one functional unit by performing at least one of lowering a supply voltage to the die, lowering a frequency of a clock signal provided by the internal clock circuitry, performing clock gating of the clock signal provided by the internal clock circuitry, performing clock throttling of the clock signal provided by the internal clock circuitry, selectively blocking clock pulses of the clock signal provided by the internal clock circuitry, disabling at least one of the plurality of functional units on the die, limiting instructions sent to at least one of the plurality of functional units on the die, and changing a behavior of at least one of the plurality of functional units on the die.

17. (Twice Amended) A computer system comprising:

at least one memory device coupled to a bus; and

at least one microprocessor coupled to the bus, the at least one microprocessor including

a die having a plurality of functional units formed thereon;

internal clock circuitry formed on the die and coupled to at least one of the plurality of functional units; and

a thermal management system located on the die, the thermal management system including

a temperature detection element formed directly on the die, the temperature detection element including at least one temperature sensor having an output;

a power modulation element formed directly on the die, the power modulation element to reduce power consumption of at least one of the functional units in response to the output of the at least one temperature sensor;

a control element formed directly on the die, the control element including at least one register to provide an enable/disable bit; and

a visibility element formed directly on the die, the visibility element to indicate a status of the output of the at least one temperature sensor.

18. (Amended) The computer system of claim 17, the at least one temperature sensor comprising:

a reference voltage source providing a reference voltage;

a programmable voltage source providing a programmable voltage proportional to a temperature of the die; and

a comparator having one input coupled via a first signal line to the reference voltage source and another input coupled via a second signal line to the programmable voltage source, the comparator to provide a signal at the output of the at least one temperature sensor in response to the programmable voltage substantially equaling the reference voltage.

19. (Amended) The computer system of claim 18, further comprising a pulse dampener coupled to the first signal line, the pulse dampener to at least partially remove electrical noise from the reference voltage.

20. (Amended) The computer system of claim 18, further comprising an analog filter coupled to the second signal line and the first signal line, the analog filter to detect voltage spikes present in the reference voltage and to add substantially identical voltage spikes to the programmable voltage.

21. (Amended) The computer system of claim 18, further comprising a digital filter coupled to an output of the comparator, the digital filter including an up-down counter to count clock pulses, the up-down counter to increment once for each clock pulse detected when the comparator output is at a first state and to decrement once for each clock pulse detected when the comparator output is at a second state.

22. (Amended) The computer system of claim 17, the control element further including at least one of a register to selectively disengage a specified portion of the thermal management system, a register to enable the thermal management system in response to an occurrence of an external event, a register to force the thermal management system active while overriding a disable bit provided by the at least one register, and a register to allow external software and hardware to enable the thermal management system.

23. (Amended) The computer system of claim 17, the visibility element including at least one of a register to indicate the status of the temperature sensor output, a register to provide a sticky bit, a counter to count a number of lost clock cycles resulting from operation of the thermal management system, and circuitry to generate an interrupt when the output of the at least one temperature sensor transitions to a different state.

24. (Amended) The computer system of claim 17, the power modulation element to reduce the power consumption of the at least one functional unit by performing at least one of lowering a supply voltage to the die, lowering a frequency of a clock signal provided by the internal clock circuitry, performing clock gating of the clock signal provided by the internal clock circuitry, performing clock throttling of the clock signal provided by the internal clock circuitry, selectively blocking clock pulses of the clock signal provided by the internal clock circuitry, disabling at least one of the plurality of functional units on the die, limiting instructions sent to at least one of the plurality of functional units on the die, and changing a behavior of at least one of the plurality of functional units on the die.

25. (Twice Amended) A method comprising:
providing an enable bit to a register to activate a thermal management system of a die;
measuring a temperature on the die with a sensor of the thermal management system;
providing a first state at an output of the sensor when the temperature is below a trip point;
providing a second state at the sensor output when the temperature equals or exceeds the trip point;
in response to the sensor output having the second state, engaging a power reduction mechanism for a specified time period to reduce power consumption of the die;
polling the sensor output after expiration of the specified time period;
engaging the power reduction mechanism for at least another one of the specified time periods if the sensor output exhibits the second state; and
halting the power reduction mechanism when the sensor output exhibits the first state.

26. (Amended) The method of claim 25, further comprising engaging the power reduction mechanism to perform at least one of lowering a supply voltage to the die, lowering a frequency of a clock signal provided by internal clock circuitry on the die, performing clock gating of the clock signal provided by the internal clock circuitry, performing clock throttling of the clock signal provided by the internal clock circuitry, selectively blocking clock pulses of the clock signal provided by the internal clock circuitry, disabling at least one of a plurality of functional units on the die, limiting instructions sent to at least one of the plurality of functional units on the die, and changing a behavior of at least one of the plurality of functional units on the die.

27. (Amended) The method of claim 25, further comprising providing an enable bit to the register from an external operating system.

31. (Twice Amended) The method of claim 25, further comprising:
incrementing an up-down counter coupled with the sensor output once for every clock pulse of the clock signal provided by the internal clock circuitry when the sensor output exhibits the first state; and
decrementing the up-down counter once for every clock pulse of the clock signal provided by the internal clock circuitry when the sensor output exhibits the second state.

32. (Amended) The method of claim 25, further comprising:
defining a plurality of trip temperatures, a highest of the plurality of trip temperatures corresponding to the trip point;
assigning a plurality of duty cycle values to the plurality of trip temperatures, one duty cycle value of the plurality of duty cycle values corresponding to at least one of the plurality of trip temperatures; and
providing a clock signal from the internal clock circuitry exhibiting the one duty cycle value in response to the temperature substantially equaling that at least one corresponding trip temperature.

33. (Twice Amended) The method of claim 25, further comprising counting a number of lost clock cycles resulting from engagement of the power reduction mechanism.

34. (Amended) An apparatus comprising:

a temperature detection element, the temperature detection element including at least one temperature sensor having an output;

a power modulation element, the power modulation element to reduce power consumption of an integrated circuit die in response to the output of the at least one temperature sensor;

a visibility element, the visibility element to indicate a status of the output of the at least one temperature sensor, the visibility element including

a register to indicate the status of the output of the at least one temperature sensor;

a register providing a sticky bit;

a counter to count a number of lost clock cycles resulting from operation of the apparatus; and

circuitry to generate an interrupt when the output of the at least one temperature sensor transitions to a different state.

E1 B2 Contd

35. (Amended) The apparatus of claim 34, further including a control element, the control element comprising:

a register to provide an enable/disable bit for the apparatus;

a register to selectively disengage a specified portion of the apparatus;

a register to enable the apparatus in response to an occurrence of an external event;

a register to force the apparatus active while overriding a disable bit provided at the enable/disable bit; and

a register to allow external software and hardware to enable the apparatus.

36. (Amended) The system of claim 34, the power modulation element to reduce the power consumption of the integrated circuit die by performing at least one of lowering a supply voltage to the integrated circuit die, lowering a frequency of a clock signal provided by internal clock circuitry on the integrated circuit die, performing clock gating of the clock signal provided by the internal clock circuitry, performing clock throttling of the clock signal provided by the internal clock circuitry, selectively blocking clock pulses of the clock signal provided by the internal clock circuitry, disabling at least one of a plurality of functional units on the integrated circuit die, limiting instructions sent to at least one of the plurality of functional units on the integrated circuit die, and changing a behavior of at least one of the plurality of functional units on the integrated circuit die.

37. (Amended) A method of forming a thermal management system on an integrated circuit die comprising:
forming a temperature detection element directly on a die;
forming a power modulation element directly on the die;
forming a control element directly on the die; and
forming a visibility element directly on the die.

38. The method of claim 37, further comprising calibrating a temperature sensor associated with the temperature detection element.

39. The method of claim 37, further comprising forming at least one functional unit on the die.

40. The method of claim 39, further comprising forming circuitry on the die common to the at least one functional unit and at least one of the temperature detection element, power modulation element, control element, and visibility element.

41. An apparatus comprising:
a first register to provide an enable/disable bit for a thermal management system on an integrated circuit die;
a second register to selectively disengage a specified portion of the thermal management system;
a third register to enable the thermal management system in response to an external event;
a fourth register to force the thermal management system active while overriding a disable bit provided by the first register; and
a fifth register to allow external software and hardware to enable the thermal management system.

42. The apparatus of claim 41, further comprising a visibility element to indicate a status of an output of a temperature sensor associated with the thermal management system.

43. The apparatus of claim 42, the visibility element comprising:
a register to indicate the status of the temperature sensor output;
another register to provide a sticky bit;
a counter to count a number of lost clock cycles resulting from operation of the thermal management system; and
circuitry to generate an interrupt when the temperature sensor output transitions to a different state.

44. The apparatus of claim 42, further comprising a power modulation element to reduce power consumption of the integrated circuit die in response to the temperature sensor output.

45. An apparatus comprising:
a register to indicate a status of an output of a temperature sensor associated with a thermal management system on an integrated circuit die;
another register to provide a sticky bit;
a counter to count a number of lost clock cycles resulting from operation of the thermal management system; and
circuitry to generate an interrupt when the temperature sensor output transitions to a different state.

46. The apparatus of claim 45, further comprising a control element including a first register to provide an enable/disable bit for the thermal management system.

47. The apparatus of claim 46, the control element further comprising:
a second register to selectively disengage a specified portion of the thermal management system;
a third register to enable the thermal management system in response to an external event;
a fourth register to force the thermal management system active while overriding a disable bit provided by the first register; and
a fifth register to allow external software and hardware to enable the thermal management system.

48. The apparatus of claim 46, further comprising a power modulation element to reduce power consumption of the integrated circuit die in response to the temperature sensor output.

Please add new claims 49-63, as set forth below.

B3 Cont'd

49. (New) The method of claim 25, further comprising providing an indication of a status of the sensor output to an external device.

50. (New) A method comprising:
activating a thermal management system of a die;
measuring a temperature on the die with a sensor of the thermal management system;
providing a first state at an output of the sensor when the temperature is below a trip point;
providing a second state at the sensor output when the temperature equals or exceeds the trip point;
engaging a power reduction mechanism for a specified time period in response to the sensor output having the second state;
polling the sensor output after expiration of the specified time period; and
halting the power reduction mechanism when the sensor output exhibits the first state.

B3 cont'd

51. (New) The method of claim 50, further comprising engaging the power reduction mechanism to perform at least one of lowering a supply voltage to the die, lowering a frequency of a clock signal provided by internal clock circuitry on the die, performing clock gating of the clock signal provided by the internal clock circuitry, performing clock throttling of the clock signal provided by the internal clock circuitry, selectively blocking clock pulses of the clock signal provided by the internal clock circuitry, disabling at least one of a plurality of functional units on the die, limiting instructions sent to at least one of the plurality of functional units on the die, and changing a behavior of at least one of the plurality of functional units on the die.

52. (New) The method of claim 50, further comprising providing an enable bit to a register from an external operating system to activate the thermal management system.

53. (New) The method of claim 50, further comprising:
incrementing an up-down counter coupled with the sensor output once for every clock pulse of a clock signal provided by internal clock circuitry on the die when the sensor output exhibits the first state; and
decrementing the up-down counter once for every clock pulse of the clock signal provided by the internal clock circuitry when the sensor output exhibits the second state.

54. (New) The method of claim 50, further comprising:
defining a plurality of trip temperatures, a highest of the plurality of trip temperatures corresponding to the trip point;
assigning a plurality of duty cycle values to the plurality of trip temperatures, one duty cycle value of the plurality of duty cycle values corresponding to at least one of the plurality of trip temperatures; and
providing a clock signal from internal clock circuitry on the die, the clock signal exhibiting the one duty cycle value in response to the temperature substantially equaling the at least one corresponding trip temperature.

B3 cont'd

55. (New) The method of claim 50, further comprising counting a number of lost clock cycles resulting from engagement of the power reduction mechanism.

56. (New) The method of claim 50, further comprising providing an indication of a status of the sensor output to an external device.

57. (New) A method comprising:
activating a thermal management system of a die;
measuring a temperature on the die with a sensor of the thermal management system;
providing a first state at an output of the sensor when the temperature is below a trip point;
providing a second state at the sensor output when the temperature equals or exceeds the trip point;
engaging a power reduction mechanism in response to the sensor output having the second state;
providing the first state at the sensor output when the temperature is below an untrip point, the untrip point less than the trip point; and
halting the power reduction mechanism in response to the first state.

B3 cont'd

58. (New) The method of claim 57, further comprising engaging the power reduction mechanism to perform at least one of lowering a supply voltage to the die, lowering a frequency of a clock signal provided by internal clock circuitry on the die, performing clock gating of the clock signal provided by the internal clock circuitry, performing clock throttling of the clock signal provided by the internal clock circuitry, selectively blocking clock pulses of the clock signal provided by the internal clock circuitry, disabling at least one of a plurality of functional units on the die, limiting instructions sent to at least one of the plurality of functional units on the die, and changing a behavior of at least one of the plurality of functional units on the die.

59. (New) The method of claim 57, further comprising providing an enable bit to a register from an external operating system to activate the thermal management system.

60. (New) The method of claim 57, further comprising:
incrementing an up-down counter coupled with the sensor output once for every clock pulse of a clock signal provided by internal clock circuitry on the die when the sensor output exhibits the first state; and
decrementing the up-down counter once for every clock pulse of the clock signal provided by the internal clock circuitry when the sensor output exhibits the second state.

61. (New) The method of claim 57, further comprising:
defining a plurality of trip temperatures, a highest of the plurality of trip temperatures corresponding to the trip point;
assigning a plurality of duty cycle values to the plurality of trip temperatures, one duty cycle value of the plurality of duty cycle values corresponding to at least one of the plurality of trip temperatures; and
providing a clock signal from internal clock circuitry on the die, the clock signal exhibiting the one duty cycle value in response to the temperature substantially equaling the at least one corresponding trip temperature.

62. (New) The method of claim 57, further comprising counting a number of lost clock cycles resulting from engagement of the power reduction mechanism.

63. (New) The method of claim 57, further comprising providing an indication of a status of the sensor output to an external device.